

5 This application claims priority from an application entitled “Multi-layer substrate having impedance-matching hole,” filed in the Korean Intellectual Property Office on January 7, 2004 and assigned Serial No. 2004-841, the contents of which are hereby incorporated by reference.

1. Field of the Invention

15

As current technology trends of various electronic devices, such as an information communication apparatus and the like, move toward smaller-size, lighter weight, and higher performance characteristics, the utilization of a multi-layer substrate becomes a necessary component for constituting an electrical system in such an electronic device. The multi-layer substrate includes a plurality of stacked metal layers on which printed circuit patterns are formed and insulating layers formed between the metal layers.

1

substrate 10 having a via hole 12. As shown in FIG. 1, the conventional multi-layer substrate 10 having the via hole 12 includes a plurality of metal layers 23, 25, 26, and 27 on which predetermined printed circuit patterns (not shown), respectively, and insulating layers 24 formed between the metal layers 23, 25, 26, and 27. When looking among the 5 metal layers, those indicated by reference numbers 23 and 27 function to transmit high-frequency signals, one metal layer 26 is a ground layer for impedance matching of high-frequency signal lines, and the other metal layer 25 functions to transmit DC and a low-frequency signal. The metal layers 23 and 27 for high-frequency signals are electrically connected with each other through a via hole 12, by a vertical plated layer 18 for 10 electrically connecting the metal layers 23 and 27 for high-frequency signals with each other is formed on an inside wall of the via hole 12.

Meanwhile, in order to reduce an impedance mismatching caused by an inductance component of the via hole 12, the multi-layer substrate 10 is fabricated so as to minimize the amount of inductance either by lengthening the diameter "d" of the via hole 12 or by 15 shortening the length "L" of the via hole 12. Also, the multi-layer substrate can be used with another method that ground holes (not shown) extended so as to be in a line with the via hole 12 are formed around the via hole 12.

However, by adjusting the diameter and the length of the via hole for impedance matching in the multi-layer substrate, there are problems introduced in that interference 20 may be caused according to the diameter of the via hole and the signal lines, such as a printed circuit pattern and the like, and also that the multi-layer substrate must ensure the minimum thickness of an insulating layer, so that it is difficult to reduce inductance by

desired amount. Also, forming a separate ground hole in the vicinity of the via hole may increase the interference problem with signal lines, such as an adjacent printed-circuit pattern.

5

SUMMARY OF THE INVENTION

Accordingly, the present invention has been made in part to solve some of the above-mentioned problems occurring in the prior art. An object of the present invention is to provide a multi-layer substrate that achieves impedance matching therein in transmitting a high-frequency signal using a via passage with an impedance matching hole.

10

To accomplish this object, in accordance with one aspect of the present invention, there is provided a multi-layer substrate comprising: a plurality of metal layers, on each of which a predetermined printed-circuit pattern is formed; and at least one insulating layer formed between the metal layers, wherein the plurality of metal layers includes: at least two high-frequency signal layers for transmitting a high-frequency signal; and at least one
15 ground layer to provide a ground for other metal layers, and wherein at least one via hole is formed through the multi-layer substrate to connect the high-frequency signal layers to each other and an impedance-matching hole extends through the ground layer so as to provide a path through which the via hole passes, and wherein a distance between the via hole and the ground layer is adjusted by the impedance-matching hole to adjust capacitance, so that
20 impedances of the multi-layer substrate are matched when a high-frequency signal is transmitted among the various layers.

BRIEF DESCRIPTION OF THE DRAWINGS

The above aspects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

5 FIG. 1 is a sectional view illustrating a construction of a conventional multi-layer substrate having a via;

 FIG. 2 is a sectional view illustrating a construction of a multi-layer substrate having an impedance-matching hole according to one preferred aspect of the present invention;

10 FIG. 3 is a sectional view of the multi-layer substrate, taken along line A-A' in FIG. 2;

 FIG. 4 is a sectional view of the multi-layer substrate, taken along line B-B' in FIG. 2;

 FIG. 5 is a construction view illustrating an electrical model of a waveguide for
15 high frequencies; and

 FIGs. 6A and 6B are graphs showing properties of a via hole and an impedance matching hole in multi-layer substrates having a thickness of 1 mm.

20

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, one preferred aspect of a multi-layer substrate having an impedance-matching hole according to the present invention will be described with reference to the accompanying drawings. In the following description of the present invention, a detailed description of known functions and configurations incorporated herein will be omitted when it may make obscure the subject matter of the present invention.

FIG. 2 is a sectional view illustrating a construction of a multi-layer substrate 30 having an impedance-matching hole according to one aspect of the present invention, FIG. 3 is a sectional view of the multi-layer substrate 30, taken along line A-A' in FIG. 2, and FIG. 4 is a sectional view of the multi-layer substrate 30 taken along line B-B' in FIG. 2. As shown in FIGs. 2 and 3, the multi-layer substrate 30 includes a hole 32 comprising metal layers 43 and 47 for high-frequency signals, a metal layer 45 for low-frequency signals and DC, a ground layer 36, insulating layers 34, the via hole 32, a ground pad 35, the impedance-matching hole 53, and a signal pad 51.

The metal layers 43, 45, 47, 35, 36, and 51 are formed as predetermined printed circuit patterns (not shown), respectively, and are stacked in the multi-layer substrate 30. Each of the metal layers 43, 45, 47, 35, 36, and 51 are configured in such a manner that the respective metal layers are stacked on the insulating layers 34, respectively. That is, the respective insulating layers 34 are formed so as to be interposed between respective metal layers 43, 45, 47, 35, 36, and 51. In addition, from among the metal layers 43, 45, 47, 35, 36, and 51, the ground layer 36 is arranged to provide a ground to the other metal layers, and at least one ground layer 36 is formed in the multi-layer substrate 30.

The via hole 32 may extend either through the multi-layer substrate 30 from one surface of the multi-layer substrate 30 or only to a predetermined length without passing through the entire multi-layer substrate 30. The metal layers 43 and 47 for high-frequency signals are electrically connected with each other through the via hole 32. In order to
 5 connect the metal layers 43 and 47 for high-frequency signals with each other, a plated layer 38 is formed on an inside wall of the via hole 32. The metal layers 43, 45, 47, 35, 36, and 51 and the plated layer 38 can be made from a material such as copper (Cu) or the like.

Meanwhile, in order to provide impedance matching in the multi-layer substrate 30, the multi-layer substrate 30 includes the matching hole 53 passing through the ground
 10 layer 36. The matching hole 53 provides a path through which the via hole 32 passes. The diameter (D_2+2l) of the matching hole 53 is adjusted in order to maintain an appropriate distance between the via hole 32 and a ground pad 35 or a ground layer 36.

In other words, both the size of the matching hole 53 and the signal pad 51 are adjusted according to a dielectric constant and a thickness of the insulating layer 34, so that
 15 capacitance components between the via hole 32 and either the ground layer 36 or the ground pad 35 can be adjusted. The capacitance components are each connected between series-connected inductance components (see FIG. 2), thereby achieving impedance matching as in a high-frequency waveguide (see FIG. 5). Note that the smaller the physical size becomes, the higher the bandwidth is achieved.

20 The signal pad 51 is located inside of the matching hole 53 and has a ring shape that extends from the outer-circumference surface of the plated layer 38 to an exterior, leaving a gap between the signal pad 51 and the ground pad 35 or the ground layer 36.

Also, the signal pad 51 is electrically connected with the plated layer 38. The signal pad 51, the ground layer 36, and the ground pad 35 are manufactured through a pattern fabricating process of a printed circuit board and generally has a very low work tolerance of 10 μm or less. Therefore, it is possible to manufacture a multi-layer substrate having the same gaps (l) between the signal pads 51 and respective corresponding ground factors 35 and 36 as designed, and is thus possible to achieve a desired capacitance.

In general, the ground pad 35 is connected with the ground layer 36 through a plurality of via holes. Sizes of the signal pad 51 and the ground pad 35 are adjusted according to a dielectric constant and a thickness of the insulating layer 34. If the via holes can be manufactured with a low work tolerance, the signal pad 51 can be omitted, and it is possible to obtain a designed capacitance by means of a distance between the via holes and the respective ground factors 35 and 36. When each layer forming the multi-layer substrate has a sufficiently small thickness, the signal pad 51 and the ground pad 35 may be formed at an interval of several layers. The ground pad 35 and the ground layer 36 may be formed on the metal layers 43 and 47 having signal lines.

FIG. 6A shows gain characteristics and FIG. 6B shows matching characteristics in a multi-layer substrate having the total thickness of 1 mm, in comparison with a first case in which only a via hole having a diameter of 200 μm is formed (0.799 nH), in a second case in which impedance is matched by using the signal pad 51 and ground pad 35. Referring to the gain characteristics shown in FIG. 6A, it is shown that the convention multi-layer substrate has more loss as a frequency increases, while the multi-layer substrate according to this aspect of the present invent shows a relatively constant gain distribution regardless

of a frequency band. Also, with the matching characteristics shown in FIG. 6B, it can be shown that the multi-layer substrate according to this aspect of the present invent shows a relatively better operation than known heretofore.

Meanwhile, the above-mentioned multi-layer substrate 30 has a form in which a plurality of unit substrates (not shown) are stacked and attached to each other. The substrates are attached to each other by using a prepreg, and the prepreg itself serves as a substrate after heat treatment. A Teflon-series substrate of the above-mentioned substrates has an excellent high-frequency characteristic. However, it is difficult to manufacture a Teflon-only prepreg because a heat treatment process with a higher temperature ($\sim 220^\circ\text{C}$) than that for normal substrates is required when the Teflon-only prepreg is connected to another layer. When a substrate is formed by attaching general Teflon-series layers with each other by means of a normal prepreg, adhesive strength is poor, so that the attached substrates may be separated. Particularly, if the substrates around the via hole are separated, the plating solution will connect the plated layer 38 to the ground factors 35 and 36, or the metal layer 45, for low-frequency signals and DC when the plated layer 38 is formed, causing a fault.

Since the signal pad 51 has been formed on a metal layer pre-attached on a Teflon-series substrate, it is possible to reduce an adhesive fault by attaching the prepreg on the signal pad, not the Teflon-series substrate. The signal pad can be formed not only for the high-frequency via, but also for another via hole for transmitting DC and low-frequency signals among other layers in order to increase adhesive strength.

As described above, according to the multi-layer substrate having an impedance-

matching hole of the present invention, the capacitance of the via hole is adjustable by varying a distance between the ground factor and the via hole in the multi-layer substrate according to the inductance of the via hole and the dielectric constant and the thickness of the insulating layer, so that impedance matching can be achieved. Moreover, the distance
5 adjustment between the ground and the via hole is performed by using the signal pad and the ground pad, so that the same capacitance as designed can be easily obtained. Also, when the signal pad is attached on the Teflon-series substrate, its adhesive strength is increased by using a normal prepreg having a low heat-treatment temperature, so that it is possible to improve the reliability of goods.

10 While the invention has been shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.